*REH*DESIGN

IDE-Interface

Manual

1. Introduction

The *REHDESIGN* IDE-Interface is a peripheral device in eurocard format, for use in ECB-bus based microcomputer systems. It contains an IDE hardisk interface (for which it is named), plus an active bus terminator for all ECB-bus signals, a parallel (Centronics) printer port, and circuitry for Reset and NMI pushbuttons. It has been designed as a supplement for single-board computers such as the *REHDESIGN* CPU280, but it can be used in all ECB-bus systems.

2. Circuit

The implementation of bus termination, centronics-interface, and Reset/NMI is simple, not to say primitive. However, the IDE-harddisk interface requires some hardware effort, unless one wants to deal with extra difficulties in the software. Harddisks with an IDE-interface transmit data in words of 16 bits, while accesses from the ECB-bus master can only transfer bytes (8 bits). Therefore each 16-bit data access has to be split into two 8-bit transactions. The simplest solution would be to separate the data on two I/O addresses, which allows the interface to identify the two halfwords by their address. This technique would not allow DMA transfers though, since DMA controllers can not alternate between two ports to access the data. This board uses another method: The splitting is done by the order of the byte accesses; that means that reading or writing to the just one I/O address alternates between odd and even half-words. This is done by toggling a flip-flop for each data access. Since all the control registers are only 8 bits wide, they don't use the toggling logic, only the data register does. Resetting the flip-flop during each access to a control register ensures that it is in the correct state when beginning a data transfer.

Nearly all of the address decoding and word-splitting is implemented using a single GAL. The remaining functions are done in simple TTL-chips. That keeps the circuit simple and the cost low.

There is a critical detail in the timing of the ECB-bus: When writing data to peripherals, the data lines become invalid approximately at the same time as when the the strobe signals change state. The (rather large) data hold time required by the IDE interface creates a real problem in this situation. To fix this problem, the IDE interface generates a synchronous write pulse using IC10 and IC11. It occurs about in the middle of the bus transaction, and ensures that the data lines stay valid long enough after the write pulse. This write pulse is used both to control the IDE harddisk and the Centronics interface. A similar pulse makes sure the upper half-word is correctly latched when reading data.

Another weak point of IDE-harddisks is their rather unstable interface behaviour. They are very sensitive to short pulses (spikes) on the address lines, even if these spikes are sufficiently far away from valid accesses. In the ECB-system used to develop this board such spikes were generated on the address lines A0 and A2 when /IORQ goes active and enables the data bus (which is physically located right next to A0 and A2). This completely confused the IDE harddisk. It seems that the only really safe solution is to add time constants, implemented here with R16, R17, C5 and C6. The spikes are attenuated by these RC-lowpass filters, and don't make it past the next input buffer. The delay caused by the lowpass filters doesn't cause any harm.

3. Parts list

IC1	GAL 20 V 8, 25 ns or faster
IC2,IC7,IC9,IC13	74 HCT 244
IC3	74 ACT 245 (or ALS)
IC4,IC11	74 HCT 32
IC5	74 HCT 139
IC6	74 HCT 373
IC8,IC12	74 HCT 374
IC10	74 HCT 74
IC14	74 HCT 123
IC15	74 HCT 00
IC16	TLC 271
T1	BD 433
T2	BD 434
T3,T4	BC 547 or similar
D1,D2,D3,D4,D5	LED 3mm red or similar
C1,C2	2 n 2 cer. LS 5
C3,C4	1 µ Ta. LS 2.5
C5,C6	47 p cer. LS 5
CK1-16,CK19-20	18x 100 n cer. LS 5
CK17,CK18	10 µ Ta. LS 2.5
R1,R11,R12	330 R
R2,R3	47 k
R4,R5	1 M
R6,R7,R8,R9	for termination of special signals
R10,R13	1 k
R14,R15	4 k 7
R16,R17	470 R
P1	50 k (trimpot 0.400" flat)
RN1	RSIL 8x 10k
RN2	RSIL 4x 10k
RN3-6	4x RSIL 8x..., for term. (220-330 R)
CN1 ECB	DIN-41612-C conn., 64 pins, rows ac
CN2 IDE	Header 40-pin
CN3 CENTR.	DB 25 S rightangle
CN3a CENTR.	Header 26-pin (Option, CN3 or CN3a)
J1 RESET	Header 1x3
J2 PDIAG	Header 1x2
J3 INIT	Header 1x2

4. Adjustment

The connector for the Centronics interface can either be a right-angle D-sub connector (for use in crates with front panels) or a header (to extend the port to any desired location).

Before using the board, the termination voltage has to be adjusted, and a few jumpers have to be selected.

A voltage of about 2.7V for the active termination has been found to be a good choice. It provides sufficient load (and therefore damping) both for high and for low signal levels. The recommended value for the resistors is in the range of 220 to 330 Ohm (should be about the same as the impedance of the bus backplane). If the CPU280 is used as the bus master, the individual resistors R6 through R9 usually don't have to be used at all.

Jumper J1 (Reset) is normally in the "upper" position, so that the signal "Reset-Out" from the bus is routed to the harddisk. Jumper J2 is usually left open (used for testing). Jumper J3 is usually left open too (who would want to reset the printer whenever the CPU is reset?).

5. GAL programming

All the central control functions of the IDE-interface are implemented in a GAL (IC1), which is a GAL 20V8.

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TITLE       IDE/CENTRONICS INTERFACE GAL IC1
AUTHOR      TILMANN REH
COMPANY     REHDESIGN
DATE        08.06.1992

; All accesses to the harddisk occur with LH = High. This means this signal
; has the opposite meaning when reading, as opposed to writing.
; For the first read access to really address the disk, one has to read the
; data register once (set LH) before the actual data transfer.

CHIP IDE PALCE20V8

CK A7 A4 A5 IORQ A6 WRP A0 A1 A2 A3 GND
OE M1 CLK LH CS0 RD16 SEL WRLO WR16 RDHI RD VCC

; Change the base address (BASE) only here! The lower nibble of the addresses
; is partially determined by hardware, and not changeable.

STRING BASE '(A7 * /A6 * /A5 * /A4)'          ; Base address 80h

STRING PARSEL '(BASE * /A3 * A2 * /A1 * A0)'  ; Centronics  Adr. x5
STRING CS1ADR '(BASE * /A3 * A2 * A1)'        ; CS1         Adr. x6..x7
STRING DATADR '(BASE * A3 * /A2 * /A1 * /A0)' ; CS0/Data    Adr. x8
STRING TFRADR '(BASE * A3 * (A2 + A1 + A0))'  ; CS0/Task    Adr. x9..xF
STRING IDEADR '(CS1ADR + DATADR + TFRADR)'    ; all IDE addresses
STRING IO '(/IORQ * M1)'                      ; I/O-Request

EQUATIONS

/CS0  = TFRADR                        ; Task file access
      + DATADR * LH                   ; Data Write MSB / Read LSB

/SEL  = (PARSEL + IDEADR) * M1        ; Board access (address only)

/CLK  = (DATADR + TFRADR) * IO        ; LH-Clock: Data & Task File

LH    := /LH * /TFRADR                ; FlipFlop: LSB/MSB Toggle
                                      ; Reset when task file access

WRLO  = DATADR * IO * /WRP * /LH      ; Data LSB write to latch
      + (TFRADR + CS1ADR) * IO * /WRP ; Transparent for all others

/WR16 = IDEADR * IO * RD              ; MSB and latched LSB to IDE

/RD16 = DATADR * IO * /RD * LH        ; Data LSB read, MSB latch
      + (TFRADR + CS1ADR) * IO * /RD  ; all others transparent

/RDHI = DATADR * IO * /RD * /LH       ; Data MSB read from Latch
```

6. Pinout ECB-bus

a	Nr	c
+5V	1	+5V
D5	2	D0
D6	3	D7
D3	4	D2
D4	5	A0
A2	6	A3
A4	7	A1
A5	8	A8
A6	9	A7
/WAIT	10	
/BUSREQ	11	IEI
	12	
(+12 V)	13	
	14	D1
-5 V	15	-12 V
2xCLK	16	IEO
	17	A11
A14	18	A10
+12 V	19	
/M1	20	/NMI
	21	/INT
	22	/WR
	23	
	24	/RD
	25	(/HALT)
	26	/RESOUT
/IORQ	27	A12
/RFSH	28	A15
A13	29	CLK
A9	30	/MRQ
(/BUSAK)	31	/RESIN
GND	32	GND

7. Software

The IDE interface occupies in total 11 addresses in the I/O address space of the ECB bus. The base address may be chosen freely in steps of 16 by appropriate GAL programming, while the lower 4 bits of the addresses must not be changed. Always the addresses x5h to xFh are used, with the standard GAL contents this means the addresses 85h to 8Fh. The particular ports have the following addresses (assuming base address 80h):

85h Centronics-Port

Writing data to this port sends the written byte to the printer port (8 bits), while reading this port returns the actual interface state. The individual bits are defined as follows:

- Bit 0 Printer: Acknowledge
- Bit 1 Printer: Paper Empty
- Bit 2 Printer: Error
- Bit 3 Printer: Select
- Bit 4 IDE Harddisk: Interrupt Request
- Bit 5 Printer: Busy
- Bit 6 Interface: Strobe Delay
- Bit 7 Interface: Composed Busy

When Polling the interface state before sending characters to the printer, bit 7 (composed busy) is to be used (0 = interface ready).

86h IDE-Harddisk Digital Output Register
87h IDE-Harddisk Alternate Status Register

These two registers are not surely existing or defined identical in different drives of different manufacturers. Before using them, the manual of the harddisk must be read! (In PC/AT's, these registers normally occupy the addresses 3F6h and 3F7h.)

88h IDE-Harddisk Data Register
89h IDE-Harddisk Error Register
8Ah IDE-Harddisk Sector Count
8Bh IDE-Harddisk Sector Number
8Ch IDE-Harddisk Cylinder Low
8Dh IDE-Harddisk Cylinder High
8Eh IDE-Harddisk Drive and Head
8Fh IDE-Harddisk Command/Status Register

These eight registers are the working registers for accessing the IDE harddisk. The contents of these registers are normally identical even with different drive types of different manufacturers (according to the so-called industry standard). However, there might me slight differences about some single bits and the usable command codes. So, reading of the individual harddisk manual is strongly recommended, too. (In PC/AT's, these registers occupy the addresses 1F0h to 1F7h.)

This manual was translated by Ralph Becker.

IDE-Interface

150792 TR

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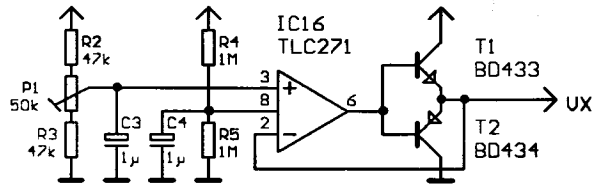
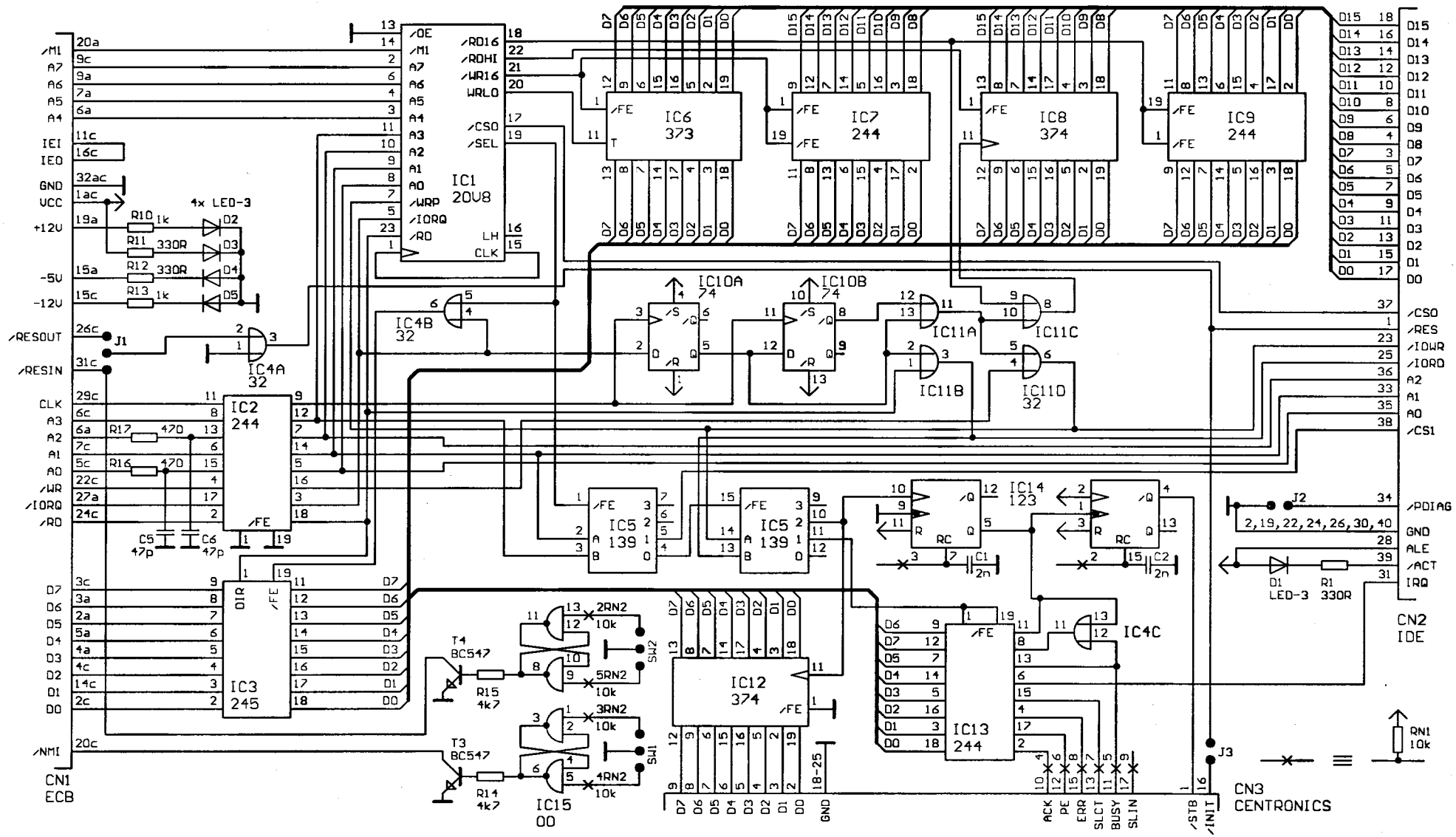
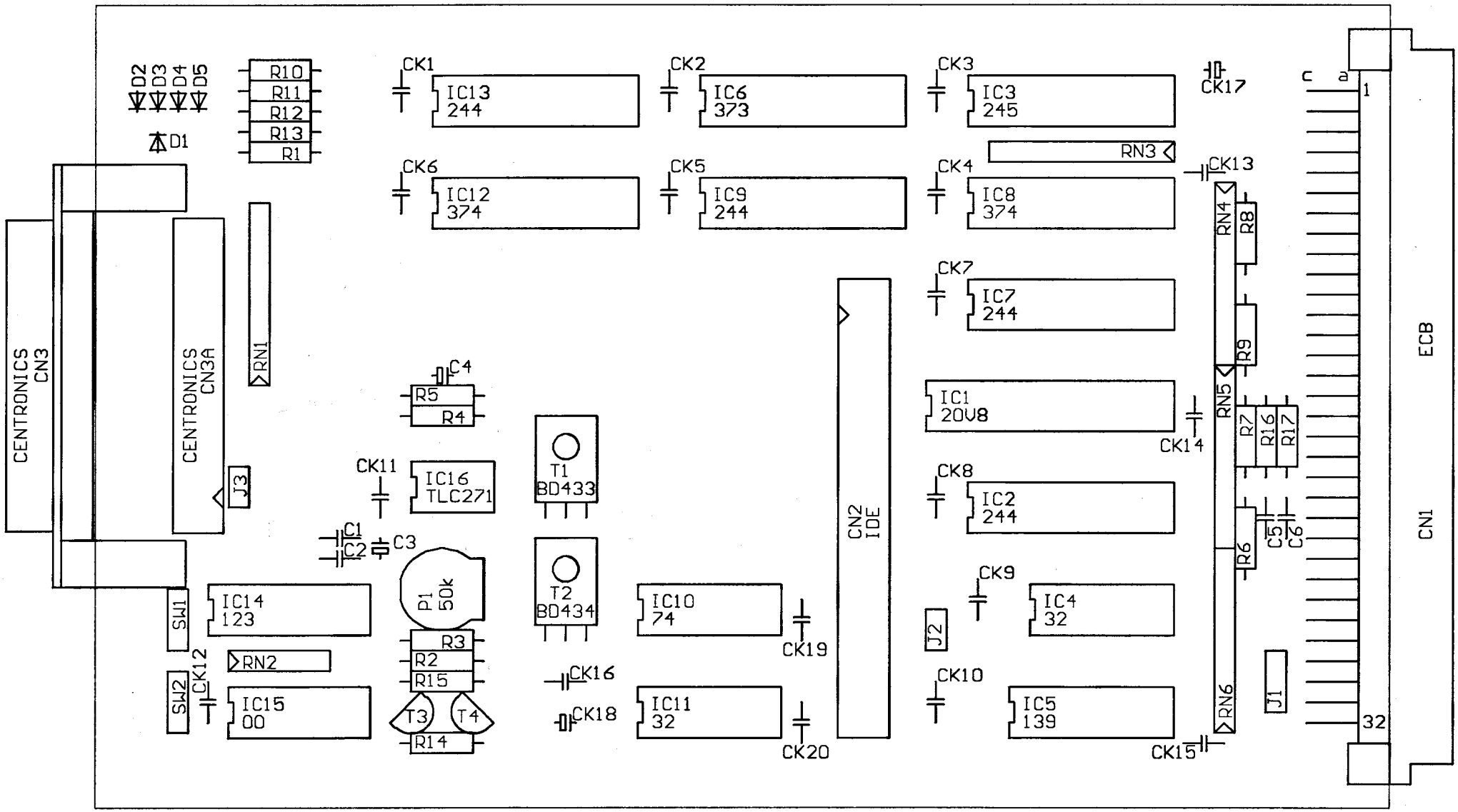


Terminierungs-Widerstände

RN3 -> D0..D7
RN4 -> A0..A7
RN5 -> A8..A15
RN6 -> MRQ,IORQ,RD,WR,M1,RFSH,CLK,2CLK
R6..R9 -> INT,NMI,WAIT,BUSRQ





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